App. No. 09/897,574
Office Action Dated September 19, 2005

REMARKS

Favorable reconsideration of this application is requested in view of the above amendments and the following remarks. Claims 1, 2, 6, 7, and 10-14 are hereby amended.

Claims 1, 6, and 11-14 are amended editorially. Claim 2 is amended to track with claim 1, from which it depends. Claims 7 and 10 are amended to track with claim 6, from which they depend. The amendment of claim 13, reciting "in an associative memory connected between the system bus and the local bus", is supported, for example, by Figure 6.

Claims 1-14 were rejected as being anticipated by West (US 6,195,730). Applicant traverses this rejection. West does not disclose or suggest a data transfer apparatus (first device) or method including a controller that fetches an address and data that are transferred between a second device and a third device that are connected only on the system bus so as to duplicate and store them in an associative memory, as required by claims 1, 11, 12, and 14. Rather, West discloses an IOP local memory (46, the rejection equates to the claimed associative memory) that does not fetch an address and data transferred between IOP n and IOP n+1 (26, rejection equates to the claimed second and third devices) that are connected to the system bus (28). In fact the IOP local memory (46) disclosed by West contains instructions and program data for an IOP microprocessor (44, rejection equates to the claimed controller) as well as data buffered for IO transfers between the IOP microprocessor (44) and an IOP local bus (42). Any address and/or data transferred between the IOP n and IOP n+1 devices are not be stored in the IOP local memory (46). The IOP local memory (46) is provided to service the IOP microprocessor (44) provided off the IOP local bus (42). See Figure 1.

Further West does not disclose a data transfer apparatus or method including a fourth device on the local bus that generates a read cycle to read data from a read address associated with the second or third devices on the system bus, where when the read address corresponds to the address stored in the associative memory, the controller transfers the corresponding data from the associative memory to the local bus, as required by claims 1, 11, 12, and 14. Rather, West discloses a storage device (22, rejection apparently equates to the now claimed fourth device)

provided off of the IOP expansion bus (36, rejection equates to the claimed local bus). However, West does not suggest that the storage device (22) is capable of generating a read cycle to read data from a read address associated with either the IOP n or IOP n+1 (26) devices. Further, the reference does not disclose or suggest that data stored in the IOP local memory (46) is transferred to the IOP expansion bus (36) for delivery to the storage device (22). As previously noted, the IOP local memory (46) is provided to service the IOP microprocessor (44) that is provided on the IOP local bus (42). See Figure 1.

West does not disclose or suggest a data transfer apparatus (first device) or method including a controller that fetches an address and data that are transferred between a second device and a third device that are connected only on the local bus so as to duplicate and store them in an associative memory, as required by claims 6 and 13. Rather, West discloses a cache memory (62, rejection equates to the claimed associative memory, controller, and buffering, accepting, and reading method steps) that is provided to buffer read data (see column 6, line 4 and Figure 2). Since the I/O adapters (48) are the only other devices connected to the IOP expansion bus (36, rejection equates to the claimed local bus), the rejection seems to equate the I/O adapters (48) to the now claimed second and third devices connected to the local bus, required by claims 6 and 13. West, however, does not disclose or suggest that the cache memory (62) transfers data requested by a fourth device off of the system bus to the system bus (28), as required by claims 6 and 13.

In fact, the cache memory (62) disclosed by West is not even provided between the local bus and the system bus, as required by claims 6 and 13. In order for data to be transferred from the cache memory (62) to a device provided off of the system bus (28), both the IOP expansion bus (36, rejection equates to the local bus) and the system bus (28) must be utilized. In contrast, the apparatus and method of claims 6 and 13 provides that data requested (corresponding to a read address associated with the second or third devices provided off of the local bus), by the fourth device provided off of the system bus, does not utilize the bandwidth of the local bus. Rather, the data is transferred directly from the associative memory to the system bus without accessing the local bus at all (see page 26, lines 14-15 and Figure 6 of the current application).

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The current invention, therefore, provides a reduction in latency of data transfer between a device provided on one bus to a device provided on another bus.

Similarly, claims 1, 11, 12, and 14 provide an apparatus and method that eliminates the need to use the system bus for transferring data to a fourth device provided off of the local bus, thereby reducing data transfer latency and load on the system bus. See page 3, lines 32-36 of the current application.

Favorable reconsideration of claims 1-14 is requested.

In view of the above, favorable reconsideration in the form of a notice of allowance is requested. Any questions regarding this communication can be directed to the undersigned attorney, Douglas P. Mueller, Reg. No. 30,300, at (612)455-3804.

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DPM:mfe

Respectfully Submitted,

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